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Demystifying Analog Circuits in Professional Audio Applications

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ABSTRACT

The past few years have seen the continuation of the shift from analog processing to digital domain processing in professional audio products. There are still several analog sections of the box that remained purely analog. Over time the performance of mixed signal components has improved significantly to the point that, once again, the weakest link in the chain could be the analog interface. The purpose of this paper is to look at a few popular analog circuits that have a direct impact on the performance of professional audio applications. The circuits are explained with mathematical demonstrations. The impact of real life implementations on the performance specifications is explored for each circuit.

1. INTRODUCTION

The electronic designs in the professional audio market have an analog line receiver of some sort at the analog inputs. Low cost applications usually have unbalanced front ends, which means that one input is "hot" the other one is the reference or ground. This type of design cannot reject common mode signals present in the signal wire as well in the ground pin. The correct line receiver for professional audio market is one that has truly balanced input. In this case the common mode signal is referenced to a third wire, the reference or ground. A good line receiver can amplify the differential signal and reject the common mode signals. The advantage of differential line receivers is that the ground wire does not carry signal and any currents flowing through the ground line do not interfere with the signal and sensitive audio circuitry at the receiving end. Often the following circuit block, after the line receiver, is an Analog to Digital Converter (ADC). The ADC inputs have particular requirements and a special driver is used to translate the large input signal swings to lower voltage levels and drive the converter inputs.

There are a few classic designs of differential line receivers. This paper presents the most commonly used topologies. Frequently, the designers reuse older circuits without paying attention to the front-end performance or not being aware of the latest technologies. The drawback could be that newer high performance ADC's that have better specifications, can exceed the performance of older line receiver topologies. Parameters that can be compromised are for instance noise, distortion and common mode rejection. A commonly used ADC driver circuit is presented and guidelines for proper design are explained.

2. LINE RECEIVERS

Three line receivers are considered for analysis, all of them designed for balanced signals and to reject common mode signals. These circuits are: the difference amplifier, the high common mode impedance amplifier for transformer-like performance and a fully differential front-end with common mode attenuation servo. In an ideal world, the first two amplifiers can achieve extremely high common mode rejection while the last one is limited by the component value selection. However, only the high common mode impedance line receiver can maintain its performance under non-ideal conditions.

2.1. Difference Amplifier

The most commonly used line receiver is the ubiquitous difference amplifier that contains an operational amplifier, two resistors connected as a pad at the non-inverting input and two resistors from output to the inverting input and then to the inverting input. A schematic of such front end is shown in Figure 1.

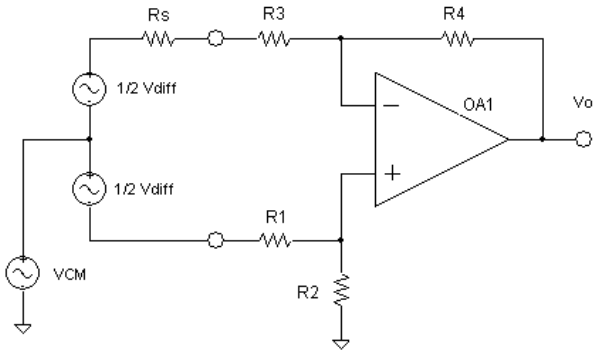

Figure 1 Difference amplifier

The main advantage of this amplifier is its simplicity, at least in theory. The realization of this circuit is an operational amplifier and four matched resistors. For unity gain all resistors are equal in value. In this case resistor networks can be used since there is a chance that all resistors match better. However, professional line levels of +24 dBu can be greater than the amplifier power supply and the unity gain amplifier can clip. To avoid clipping, +/- 20 V power supply rails are required, which can dissipate a lot of power. For lower power supply rails, a gain of -6dB or -3 dB is needed. The most common line receiver, and not necessarily the best choice, is the -6 dB version.

The common mode rejection performance varies tremendously due to inherent resistor variation. The Common Mode Rejection Ratio (CMRR), for the -6dB version, is better than 37.5 dB if 1 % resistors are used and better than 57.5 dB for 0.1 % resistors. However, Printed Circuit Board (PCB) copper trace resistance, operational amplifier terminal resistance and other factors make the discrete implementation very difficult. Using better matched discrete resistor will not improve the CMRR because of the unpredictable resistive errors on the board. The only solution to increase the CMRR is to use specialized integrated circuits that have the matched resistors on the die. These resistors are made of thin film materials, such as NiCr or SiCr, which are very stable with temperature and over time. The thin film resistors are fine trimmed using laser trimming to match down to 0.005 %, or 90 dB of CMRR. This kind of performance is almost impossible (or very expensive) with discrete components. The CMRR, in decibels or dB, of the difference amplifier can be calculated as follows [1]:

$$CMRR = 20 * \log\left(\frac{1+gain}{\sum\frac{\Delta R}{R}}\right) \quad (1)$$

where the gain and resistor error are defined as:

$$gain = \frac{R_2}{R_1} = \frac{R_4}{R_3} \quad (2)$$

$$\sum\frac{\Delta R}{R} = \sum_{n=1..4}\frac{\Delta R_n}{R_n} \quad (3)$$

Equation (3) represents the total resistor error of all four resistors as a sum of individual resistor error.

The CMRR performance of the difference amplifier is very good under ideal conditions, that is, if the lines connecting to the line receiver are truly balanced. A balanced line means that the impedances of the two wires driving the line receiver are equal at least across the audio frequency spectrum [11]. This is the ideal condition under which the difference amplifier can hold its CMRR performance.

What happens if the lines are not balanced ?

A 10 Ω imbalance drops the CMRR performance by 25 dB. Worse, if the line receiver connects to an unbalanced output driver that usually has a 100 Ω series resistor in the signal path, the CMRR performance drops by 45 dB. In this case the end user has to be very careful in choosing the cables and the interconnects. In live sound applications is very difficult to control the quality of the cables and matching of outputs and inputs. In order to improve the situation, the designer has a few choices. One solution is to increase the common mode impedance. The penalty is that the total output noise is going to increase as well and finally it reduces the dynamic range. The common mode impedance can be calculated as follows (refer to Figure 1):

The current into the non-inverting input is:

$$I_{R1} = \frac{V_{CM}}{R_1 + R_2} \tag{4}$$

The current into the inverting input is:

$$I_{R3} = \frac{V_{CM} * R_1}{(R_1 + R_2) * R_3} \tag{5}$$

Finally the common mode impedance is calculated as:

$$Z_{CM} = \frac{V_{CM}}{I_{R1} + I_{R3}} = \frac{R_1 + R_2}{1 + \frac{R_1}{R_3}} \tag{6}$$

If R1 is not equal to R3, see equation (4) and (5), then the common mode currents into the two inputs are not equal either. In this case even a balanced line cannot prevent the common mode signal to be transformed to a balanced signal that cannot be rejected by the amplifier. Therefore, it's good practice to have R1 equal to R3 and R2 equal to R4. In this case, the common mode impedance is:

$$Z_{CM} = \frac{1}{2} * (R_1 + R_2) \tag{7}$$

For most -6 dB audio line receivers available on the market today the common mode impedance is 9 kΩ [1][2][3]. Not a whole lot.

There are other variations of the basic difference amplifier that extend the input common mode range to hundreds of volts while increasing the common mode impedance to hundreds of kΩ. This can be done by replacing resistor R4 in Figure 1 with a "T" resistor network. One end of the "T" network is connected to the amplifier output, the other end to the inverting input of the operational amplifier and finally the bottom leg connects to ground. This type of circuit requires an operational amplifier with very high open loop gain since it operates at very high noise gain. The noise gain is the gain seen from the non-inverting input of the operational amplifier. The drawback of high noise gain is low loop transmission gain. The amplifier distortion and frequency bandwidth is directly proportional to the remaining loop gain. Thus, the circuit bandwidth is reduced and the distortion at high frequencies is not very good.

Best line receiver gain for highest dynamic range

The common question that a designer is faced with is how to choose the line receiver gain to maximize the dynamic range. The maximum input level for professional equipment is 24 dBu (or +4 dBu plus 20dB of headroom) and the typical power supply inside the unit is +/- 15V. Browsing through the data sheets of such amplifiers [1][2][3] one can determine that the maximum output level is 21.5 dBu. The output noise also varies from manufacturer to manufacturer especially for unity gain amplifiers. The dynamic range measured as signal to noise ratio is the maximum output level in [dB] minus the output noise floor of the amplifier, also in [dB].

Line Receiver Gain	Manufacturer 1		
	Max output	Noise floor	Dynamic range
0 dB	21.5 dBu	-103 dBu	124.5 dB
-3 dB	21.0 dBu	-105 dBu	**126.0 dB**
-6 dB	18.0 dBu	-106 dBu	124.0 dB
	Manufacturer 2		
0 dB	21.5 dBu	-100 dBu	121.5 dB
-3 dB	N/A	N/A	N/A
-6 dB	18.0 dBu	-106 dBu	124.0 dB

Table 1 Dynamic range vs. line receiver gain for typical +/- 15V power supply and +24 dBu maximum input level.

The table above shows the maximum signal to noise dynamic range for two Integrated Circuit (IC) manufacturers and different gains. The best dynamic range is highlighted in bold face. Interestingly enough, the designer can increase the dynamic range by almost 2 dB by using the -3 dB line receiver. Fortunately, such an amplifier is available from at least one IC manufacturer [3].

2.2. High CM Impedance Amplifier

The difference amplifier presented in the previous chapter has the main disadvantage that the common mode impedance is very low and its performance quickly degrades in real life application. Users that are faced with large common mode signals use transformers to couple between signal processing units and other equipment. The transformer has extremely high common mode input impedance and offers very good common mode rejection at low frequencies. The drawback of the transformer is that the high frequencies common impedance, and therefore common mode rejection, is not as high as at low frequencies due to stray capacitances. Another issue is that the distortion at low frequencies is not that great either. The transformers usually add a "color" to the sound that it's not always desirable. Finally, transformers are bulky, heavy and the high performance ones are expensive.

The solution to afore mentioned issues came in the form of an ingenious design [4], that exploits the benefits of the bootstrap and instrumentation amplifiers, see Figure 4. It is worth mentioning that this design is protected by US Patent 5,568,561. The bootstrap is an old technique to increase the input impedance of an amplifier. The input impedance at the amplifier input is connected between the input and instead of connecting the other end to ground, it's connected to a replica of the input signal. Essentially, the bootstrap is a positive feedback system. To keep the system stable, the non-inverting amplifier that copies the input signal has to have a gain of less than one.

The basic schematic of the bootstrap circuit is shown in Figure 2.

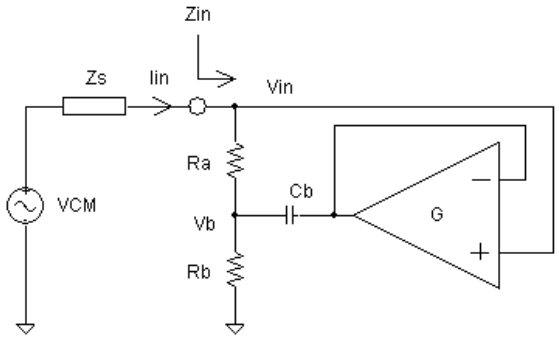

Figure 2 Bootstrap amplifier.

The theory behind the bootstrap amplifier can be explained by determining the equivalent input impedance at the input. Summing all the currents at node Vb we have the following equation (refer to Figure 2):

$$\frac{V_{in}-V_b}{R_a}+\left(V_{in}*G-V_b\right)*sC_b=\frac{V_b}{R_b} \qquad (8)$$

Equation (8) is solved for Vb as follows:

$$V_b=R_b*\frac{1+sC_bR_a*G}{\left(R_a+R_b\right)+sC_bR_aR_b} \qquad (9)$$

Input current Iin is calculated from the following equation:

$$I_{in}=\frac{V_{in}-V_b}{R_a} \qquad (10)$$

Finally, the input impedance is calculated by dividing the input voltage, Vin, to the input current, Iin, as follows:

$$Z_{in} = \frac{V_{in}}{I_{in}} = (R_a + R_b) * \frac{1 + sC_b \dfrac{R_a R_b}{R_a + R_b}}{1 + sC_b R_b * (1 - G)} \quad (11)$$

The input impedance is the sum of the two input resistors multiplied by a frequency dependent factor. The frequency dependent factor has a zero and a pole in the transfer function. Since (1-G) is very small, the zero frequency is lower than the pole. Please note that if the gain of the amplifier is considered unity, G = 1, then the input impedance transfer function has only one zero, which means that the input impedance rises with frequency without limit. This is not a realistic assumption. Although the gain of the amplifier is very close to unity, e.g., G = 0.999, it is important to consider it.

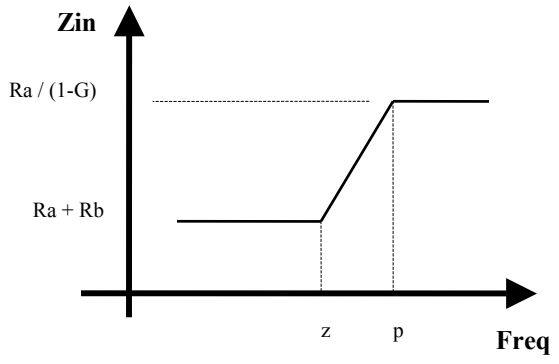

Figure 3 Input impedance of bootstrapped amplifier vs. frequency.

The zero and pole frequencies can be extracted from equation (11) as follows:

$$f_z = \frac{1}{2\pi * C_b \dfrac{R_a R_b}{R_a + R_b}} \quad (12)$$

$$f_p = \frac{1}{2\pi * C_b R_b * (1 - G)}$$

The minimum and maximum input impedance can be extracted from equation (11) at zero and infinite frequencies.

$$Z_{in}\big|_{f=0} = R_a + R_b$$
$$Z_{in}\big|_{f=\infty} = \frac{R_a}{1 - G} \quad (13)$$

For a set of typical resistor, capacitor and amplifier values, such as, Ra = 12 kΩ, Rb = 24 kΩ, Cb = 220 μF and G = 0.999 we get the following zero, pole and impedances:

$$f_z = 0.09Hz$$
$$f_p = 30Hz$$
$$Z_{in}\big|_{f=0} = 36k\Omega \quad (14)$$
$$Z_{in}\big|_{f=\infty} = 12M\Omega$$

One concern with the bootstrap technique is that if a capacitive source impedance is connected to the input, then the common mode transfer function could peak resulting in gain at the resonant frequency. This behavior can void the advantages of the bootstrap reducing the common mode rejection at the peaking frequency. It will be shown that by ignoring the actual closed loop gain, which is less than one, of the bootstrap amplifier, the results are not correct and that there is a tremendous difference between the ideal model and a more realistic amplifier gain closer to unity.

Let's assume that the source impedance Zs in Figure 2 is of capacitive nature. In this case:

$$Z_s = \frac{1}{sC_s} \quad (15)$$

The transfer function can be calculated as follows:

$$H(s) = \frac{V_{in}}{V_{CM}} = \frac{Z_{in}}{Z_{in} + Z_s} \quad (16)$$

Combining equations (11), (15) and (16) we can calculate the transfer function as:

$$H(s) = \frac{\alpha * s \dfrac{\omega_{CM}}{Q} + s^2}{\omega_{CM}^2 + s \dfrac{\omega_{CM}}{Q} + s^2} \quad (17)$$

In equation (17) we have the following definitions:

The common mode resonant frequency ω_{CM} is defined as:

$$\omega_{CM} = \frac{1}{\sqrt{C_s C_b R_a R_b}} \quad (18)$$

The "Q" factor is defined as:

$$Q = \frac{\sqrt{R_a R_b} * \sqrt{\frac{C_b}{C_s}}}{(R_a + R_b) * \left[1 + \frac{C_b}{C_s} * \frac{R_b * (1-G)}{R_a + R_b}\right]} \quad (19)$$

The α factor is defined as follows:

$$\alpha = \frac{1}{1 + \frac{C_b}{C_s} * \frac{R_b * (1-G)}{R_a + R_b}} \quad (20)$$

The common mode transfer function with a capacitor connected at the input is a combination of a band pass and a second order high pass filters. The α factor is the gain (or loss) of the band pass filter due to the finite closed loop gain of the common mode amplifier. Please note that an ideal closed loop gain of one makes α = 1.

From equation (17) we can calculate the transfer function value at the resonant frequency ω_{CM} .

$$s = j\omega_{CM}$$
$$H(j\omega_{CM}) = \alpha + jQ \quad (21)$$

and the absolute value of the transfer function is:

$$|H(j\omega_{CM})| = \sqrt{\alpha^2 + Q^2} \quad (22)$$

Equation (22) is evaluated for peaking at the resonant frequency. The transfer function is tested if it can be less than one.

$$|H(j\omega_{CM})| \le 1$$
$$\alpha^2 + Q^2 \le 1 \quad (23)$$

Equations (19) and (20) are substituted in (23). Then the equation is rearranged to solve for the capacitor ratio Cb / Cs as follows:

$$\frac{C_b}{C_s} \ge \frac{R_a - 2*(1-G)*(R_a + R_b)}{R_b * (1-G)^2} \quad (24)$$

Term (1-G) is of the order of 0.001 or smaller, and resistors Ra, Rb are close in value. Thus, equation (24) can be simplified as follows:

$$\frac{C_b}{C_s} \ge \frac{R_a}{R_b * (1-G)^2} \quad (25)$$

Note that if the common mode amplifier is considered ideal with a gain of one, then the right hand term in equation (25) is infinite. This means that the common mode transfer function is always going to peak at the resonant frequency ω_{CM} . However, in the real model of the common mode amplifier there is a finite ratio of capacitors for which the common mode transfer function does not peak.

One possible case is if the input of the bootstrapped amplifier is left open and the input connector has a capacitor connected to ground as an Radio Frequency (RF) filter. Usually these capacitors are in the order 100 pF. Considering the typical values exemplified above in the text, to avoid peaking the capacitor ratio has to be greater than:

$$\frac{C_b}{C_s} \ge \frac{12k\Omega}{24k\Omega * (1-0.999)^2} = 0.5 * 10^6 \quad (26)$$

Typically Cs is 100 pF, which means that Cb has to be greater than 50 µF. The recommended value for Cb is 220 µF, therefore there is no danger of peaking. This is especially important since the common mode resonant frequency is in the range of interest. The resonant frequency can be calculated from equation (18) as follows:

$$f_{CM} = \frac{1}{2\pi * \sqrt{C_s C_b R_a R_b}} \qquad (27)$$

Using the same values exemplified in the text the resonant frequency is 63 Hz.

The table below shows the error in the common mode transfer function between the ideal model, where the common mode amplifier gain is one, and the more realistic model, where the common mode amplifier gain is less then one. The error is computed at the resonant frequency of the common mode amplifier. The numbers in the table below were calculated using formulae (19), (20), (23) and (27). The component values are Cb = 220 µF, Cs = 100 pF, Ra = 12 kΩ and Rb = 24 kΩ.

Parameter	Ideal CM loop gain G = 1	Real CM loop gain G = 0.999
f_{CM}	63 Hz	63 Hz
α	1	$6.81*10^{-4}$
Q	699	0.476
$\lvert H(j\omega_{CM})\rvert$	**+57 dB**	**- 6.5 dB**

Table 2 Absolute value of CM transfer function calculated using two models for the common mode amplifier. See text for component values.

Table 2 shows that ignoring one thousandth in the amplifier gain the results at resonant frequency can differ by more than 60 dB !!!

Another possible case is when the input of the bootstrapped amplifier is "ac" coupled with a "dc" blocking capacitor. A typical value for the coupling capacitor is 10 to 22 µF. In this case peaking is possible but the resonant frequency is 0.2 Hz or lower, well below the frequency range of interest. This low resonant frequency can generate a common mode "dc" pop that can take a few good seconds to settle. However, the difference amplifier, which follows the bootstrapped amplifier, can reject the "dc" transient, refer to Figure 4.

Another note about the stability of the common mode closed loop is that although it is positive feedback its open loop gain is always less than one, especially at low frequencies where under special circumstances peaking may occur. Also, the positive feedback is always less than the negative feedback at operational amplifiers OA1 and OA2.

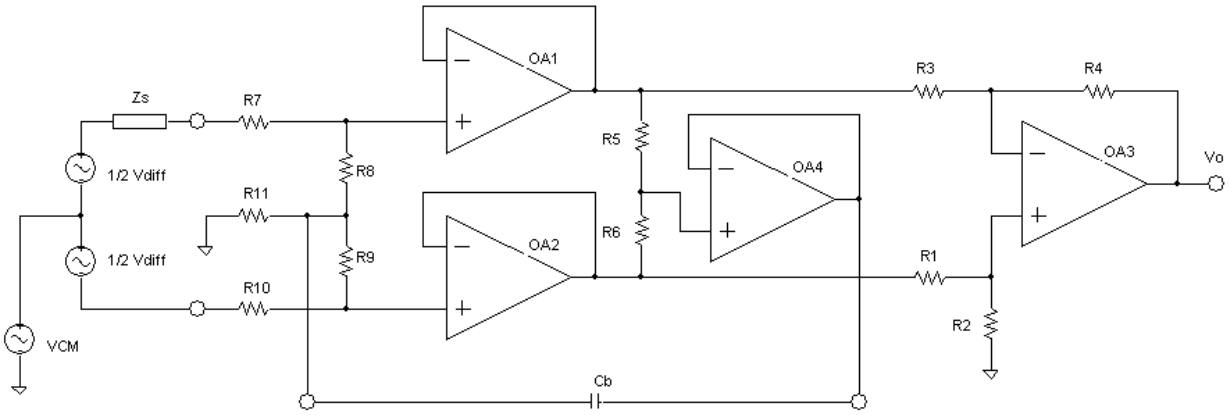

Figure 4 High common mode impedance line receiver.

Figure 4 shows the entire line receiver schematic. Operational amplifiers OA1 and OA2 are the input buffers and OA4 is the common mode amplifier. OA1 and OA2 buffer both the differential and the common mode signals. The difference amplifier OA3 and the resistor network around it, R1 through R4, reject the common mode. OA4, resistors R5 and R6 extract the

common mode signal and buffer it back to the input to close the bootstrap loop.

The circuit in Figure 4, with typical values as exemplified in the text, exhibits 48 kΩ of differential impedance, while the common mode impedance is better than 10 MΩ. Practically, any impedance unbalance at the input does not alter the CMRR performance. This way, transformer-like performance is obtained while maintaining very good distortion performance at low frequencies. If circuit in Figure 4 is integrated on silicon, then the common mode rejection at high frequencies is highly improved due to tight control of stray capacitance on the die.

2.3. Differential Amplifier with CM Attenuation

Another popular line receiver is the circuit shown in Figure 5. It's a fully differential amplifier that can be followed by a difference amplifier or by an ADC [5]. Operational amplifiers OA1 and OA2 buffer the differential and reduced common voltage signals. Operational amplifier OA3 is the common mode loop servo amplifier. At a glance, this circuit might look similar to the high common mode impedance line receiver presented in the previous chapter that uses bootstrap. Some designers are tempted to believe that OA3 is a bootstrap amplifier. However, the differential amplifier in Figure 5 has a fundamentally different mode of operation.

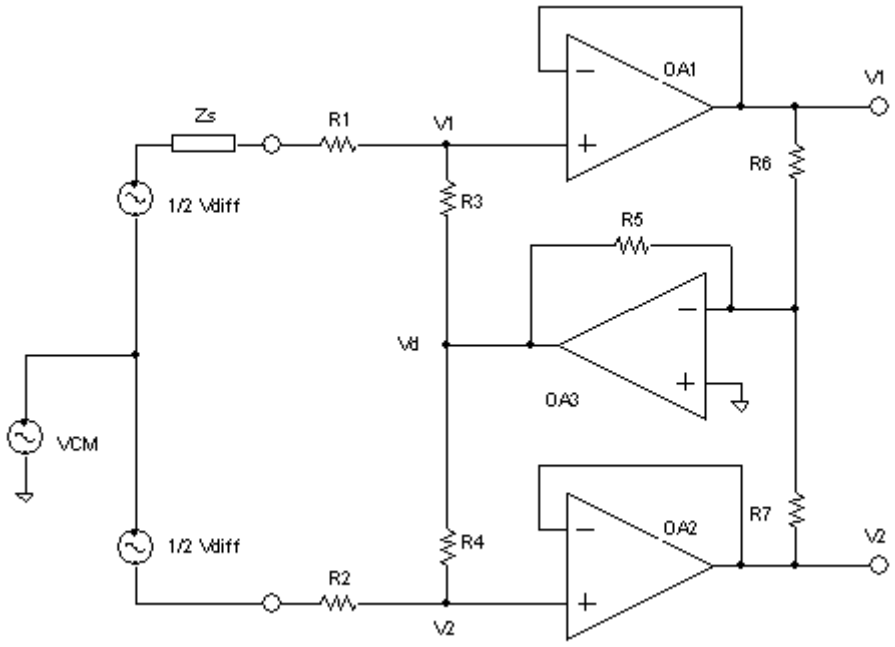

Figure 5 Differential amplifier with CM rejection

Operational amplifier OA3 senses the output common mode voltage, buffered by OA1 and OA2, and outputs a voltage of opposite polarity to the input common mode voltage at node Vd. The voltage at node Vd is such that nodes V1 and V2 are kept as close as possible to ground when common mode signal is applied at the input. Thus, the common mode voltage is attenuated. If V1 and V2 are always kept at virtual ground for common mode signals, the common mode impedance can be easily calculated as R1 in parallel with R2. Because the voltage at node Vd is of opposite polarity to the input common mode voltage, OA3 actually decreases the common mode input impedance by a factor of (1 + (R3/R1)). This mode of operation is exactly the opposite of bootstrap. Also, it will be shown that the common mode attenuation is finite and it is dependent by the component value selection. A subsequent stage connected after this line receiver, such as a difference amplifier or an ADC, can reject the common mode voltage even more. This topology is usually recommended to drive ADC's, which have additional common mode rejection [5].

The resistor network at the input, R1, R2, R3 and R4 attenuates the differential signal as well, and

configurations of -3 dB or -6 dB can be achieved. Unity gain configuration is not possible with this circuit since the common mode attenuation is dependent on resistors R1 and R2. The differential input impedance is the sum of all input resistors R1, R2, R3 and R4. Typically R1 is equal to R2 and R3 is equal to R4.

The -6 dB configuration requires that all input resistors to be equal. In order to compare it to the -6 dB difference amplifier, that has a typical 24 kΩ differential input impedance and 9 kΩ common mode input impedance, we need to set all input resistors to 6 kΩ. This way, the differential input impedance is similar. But, the common mode impedance is only 3 kΩ, about three times lower than the difference amplifier.

The common mode attenuation can be calculated by writing the following set of equations (refer to Figure 5):

$$\begin{aligned} V_1 &= \left(V_{CM} - V_d\right) * \frac{R_3}{R_1 + R_3} + V_d \\ V_d &= -V_1 * \frac{R_5}{R_6} \end{aligned} \qquad (28)$$

The set of equations in (28) can be solved for V1 as follows:

$$V_1 = \frac{V_{CM}}{1 + \frac{R_1}{R_3} * \left(1 + \frac{R_5}{R_6}\right)} \qquad (29)$$

Finally, assuming that the differential amplifier is symmetric, the CMRR is calculated as the ratio of the differential gain divided to the common mode gain as follows:

$$CMRR = \frac{\left(\frac{V_1 - V_2}{V_{diff}}\right)}{\left(\frac{V_1}{V_{CM}}\right)} \qquad (30)$$

The differential gain is the attenuation of the input resistor network, R3 / (R1 + R3). Substituting equation (29) in (30) we can calculate the common mode rejection as follows

$$CMRR = 1 + \frac{\frac{R_5}{R_6}}{1 + \frac{R_3}{R_1}} \qquad (31)$$

Since R1 and R3 are close in value, the common mode rejection relies on the ratio of R5 to R6, which is half the closed loop gain of operational amplifier OA3. In order to get decent CMRR, this gain has to be at least 40 dB. As explained in a previous paragraph, the available loop gain of OA3 is reduced by its closed loop gain increasing distortion and reducing the bandwidth. The distortion is not really an issue here but the bandwidth could be. Operational amplifier OA3 requires very high open loop gain. Let's say we chose an operational amplifier with an open loop gain of 80 dB and the ratio of R5 / R6 is set for 60 dB gain. If R6 = R7, in Figure 5, the closed loop gain of OA3 is 2 * (R5 / R6), in this case 66 dB. The available loop gain is only 14 dB. Typically the dominant pole in the open loop transfer function is less than 10 Hz. This choice of operational amplifier yields a usable bandwidth of only 50 Hz. An operational amplifier with an open loop gain of 100 dB can increase the bandwidth to approximately 500 Hz.

The topology presented here is a typical circuit that works great in the designer's notebook, pretty well in the engineering lab under controlled environment and poorly in real life applications. The first major issue is the very low common mode impedance. A 100 Ω unbalance at the input, assuming ideally matched components in the circuit, drops the common mode rejection to only 35 dB. The second major issue is that the common mode rejection is dependent on the matching of the input resistor network, R1 through R4. The only solution to get matched resistors is to make an integrated circuit that incorporates the resistors and the operational amplifiers. As of today there is no such integrated circuit available. Even if there would be an integrated circuit solution, the common mode attenuation is proportional to the closed loop gain of OA3. The bandwidth of the common mode servo loop is also limited which makes this circuit not suitable for rejecting high frequency common mode signals.

2.4. Summary of line receivers

The difference and the high common mode input impedance amplifiers were presented with differential input and single ended output. However, they can be

configured for differential output as well to drive the input of an ADC [12]. The table below shows typical performance of line receivers presented in the paper.

Parameter	Difference amplifier	High CM impedance amplifier	Differential amplifier with CM rejection
Differential Input Impedance	24 kΩ to 50 kΩ	48 kΩ	24 kΩ to 50 kΩ
Common Mode Input Impedance	9 kΩ to 25 kΩ	10 MΩ	3 kΩ to 6 kΩ
Ideal CMRR	90 dB	90 dB	40 dB to 60 dB
CMRR with an 100 Ω unbalance at the input	45 dB to 54 dB	90 dB	35 dB

Table 3 Typical common mode performance of line receivers presented in the paper

3. ADC DRIVER CIRCUIT

A typical ADC application circuit requires a filter capacitor connected between the inputs of the converter. The typical value of this capacitor is 2.7 nF [6][7][8], which means that in the case of a differential input each side has to drive the equivalent of 5.4 nF. Also, most of the ADC's have low power supplies voltages, usually +5V and ground or +/- 5V (older models). Audio ADC's have CMOS switches at the very input that work at relatively high frequencies. The switching current in the stray CMOS capacitor is in the order of milliamps at megahertz switching speeds. All of the above set the ADC driver requirements as follows:

- Driver has to attenuate professional line levels to ADC's limited input range, typically from about 20 Vrms down to about 2 Vrms.
- Driver has to drive a significant capacitive load, at least 5.4 nF.
- Driver should be able to absorb high frequency current spikes.
- Driver should have very low output impedance in order to maintain the ADC distortion at a minimum.

This paper addresses the requirement of driving capacitive loads and explains a widely used driver circuit with design guidelines for component values.

The circuit in Figure 6 shows an ideal operational amplifier, OA1, which is driving a capacitive load, CL. The open loop gain of the operational amplifier is A(s). The resistance in series with the output, r_0, models the output resistance of the amplifier. At low frequencies this resistance is very small and it doesn't matter. However, at higher frequencies where the loop gain of the operational amplifier is lower, the output impedance starts to rise and it adds yet another pole in the negative feedback of the amplifier. The gain of the circuit in Figure 6 is set by the feedback network beta (β). The theory remains the same for any gain, the loop gain decreases even more if there is less negative feedback.

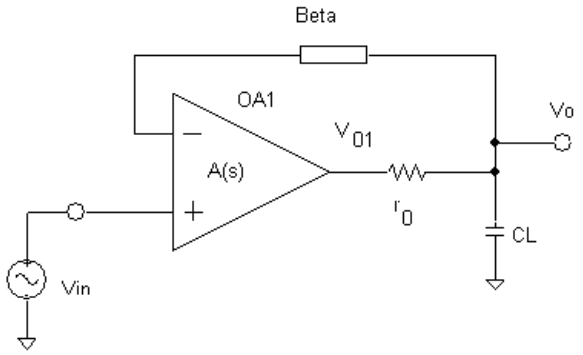

Figure 6 Typical operational amplifier driving a capacitive load

The next figure, Figure 7, shows the relationship between the open loop gain, closed loop gain and loop gain (also known as loop transmission). If low closed loop gains are used then there is plenty of loop gain.

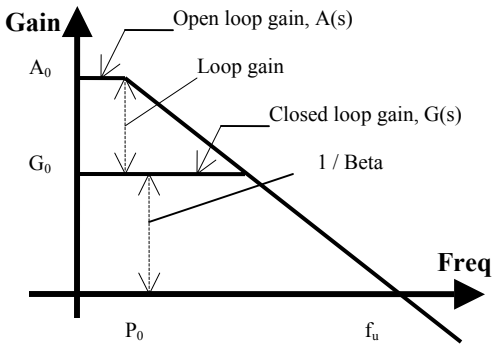

Figure 7 Operational amplifier open loop gain, closed loop gain and loop transmission

The stability of the operational amplifier can be studied by analyzing the characteristics of the loop transmission. The relationship between all the gains in Figure 7 is shown in the following equation [9]:

$$G(s) = \frac{A(s)}{1+\beta * A(s)} \qquad (32)$$
$$LT(s) = \beta * A(s)$$

The loop transmission is the product $\beta * A(s)$. β is the feedback factor that sets the closed loop gain. For unity gain $\beta = 1$. The open loop gain function, A(s), is modeled by a one-pole transfer function as shown in the next equation [9]:

$$A(s) = \frac{A_0}{1+\frac{s}{p_0}} \qquad (33)$$

Replacing A(s) as shown in equation (33) in equation (32), the closed loop gain becomes:

$$G(s) = \frac{A_0}{1+\beta * A_0} * \frac{1}{1+\frac{s}{p_0 * (1+\beta * A_0)}} \qquad (34)$$

The closed loop gain bandwidth is the open loop pole multiplied by the factor $(1+\beta * A_0)$. The higher the open loop gain the higher the closed loop bandwidth, and the higher the closed loop gain the lower the closed loop bandwidth.

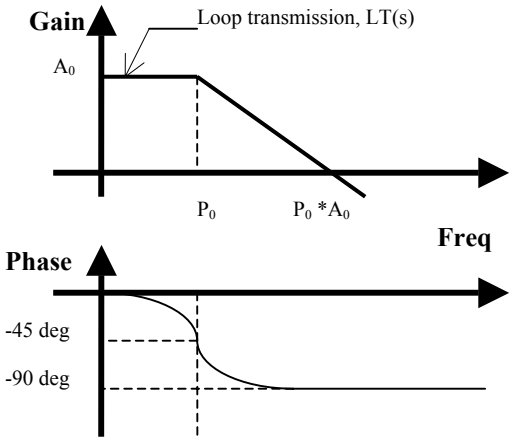

Figure 8 Operational amplifier loop transmission gain and phase

Figure 8 shows the loop transmission gain and phase. When the phase reaches -180 deg, the overall feedback becomes positive and the operational amplifier oscillates. As a rule of thumb, the phase should be greater than -135 deg, ideal -90 deg [10].

The problem: driving capacitive loads

With the above notes in mind we'll proceed to compute the effect of the load capacitor, CL, on the loop transmission of the operational amplifier. In order to simplify the equations we set $\beta = 1$. From Figure 6 we can determine the following equations:

$$V_{01} = (V_{in} - V_0) * A(s)$$
$$V_0 = \frac{V_{01}}{1+sr_0C_L} \qquad (35)$$

Solving the above equations, we can determine the closed loop gain as follows:

$$G(s)=\frac{V_0}{V_{in}}=\frac{\frac{A(s)}{1+sr_0C_L}}{1+\frac{A(s)}{1+sr_0C_L}} \quad (36)$$

We make the following notation:

$$p_{CL}=\frac{1}{r_0C_L} \quad (37)$$

Substituting (33) and (37) in (36), the loop transmission can be calculated as follows:

$$LT(s)=\frac{A_0}{\left(1+\frac{s}{p_0}\right)*\left(1+\frac{s}{p_{CL}}\right)} \quad (38)$$

Note that the load capacitor and the output series resistance form an additional pole in the frequency response. The absolute value of the loop transmission can be calculated from (38) as follows:

$$\left|LT(j\omega)\right|=\frac{A_0}{\sqrt{1+\frac{\omega^4}{(p_0p_{CL})^2}+\omega^2*\left(\frac{1}{p_0^2}+\frac{1}{p_{CL}^2}\right)}} \quad (39)$$

Equation (39) can be solved for $\left|LT(j\omega)\right|=1$ and the frequency at which the loop transmission gain drops to one can be found as follows:

$$\omega_{LTu}=\sqrt{p_0p_{CL}A_0} \quad (40)$$

The location of ω_{LTu} is not very well determined. It could be between the two poles $p_0<\omega_{LTu}<p_{CL}$ or it could be greater than the second pole $p_0<p_{CL}<\omega_{LTu}$. The location of the unity frequency is important in determining the stability of the operational amplifier. We need to look at the phase of the loop transmission. The phase can be determined from equation (38) as follows:

$$\varphi=tg^{-1}\left(\frac{-\omega\left(\frac{1}{p_0}+\frac{1}{p_{CL}}\right)}{1-\frac{\omega^2}{p_0p_{CL}}}\right) \quad (41)$$

If we assume that:

$$p_0<<p_{CL} \quad (42)$$

then, at frequency $\omega=p_0$ the phase is:

$$\varphi=tg^{-1}(-1)=-45\,\text{deg} \quad (43)$$

The phase margin at the loop transmission unity gain frequency can be calculated by substituting equation (40) in equation (41) and considering equation (42).

$$\varphi=tg^{-1}\left(\sqrt{\frac{p_{CL}}{p_0A_0}}\right) \quad (44)$$

Note that the square root term in parenthesis, in equation (44), is always positive. Since the phase is already below -45 deg, and because we are looking at frequencies above pole p_0, it means that the phase can be anywhere in the range of $\varphi\in(-90\,\text{deg}\div-180\,\text{deg})$. In other words it could be ok if it's closer to -90 deg but it could be trouble if it's closer to -180 deg. Let's take a closer look.

If the loop transmission unity gain frequency is between the poles, $p_0<\omega_{LTu}<p_{CL}$, it means that the following statement is true: $p_0A_0<p_{CL}$. This can be determined from equation (40). In this case the square root term in parenthesis, in equation (44), is positive and greater than one. Therefore the phase can be in the range of $\varphi\in(-90\,\text{deg}\div-135\,\text{deg})$. That is good, it means that the operational amplifier is stable. In Figure 9 there is a graphical representation of the pole locations and phase with respect to loop transmission unity gain frequency.

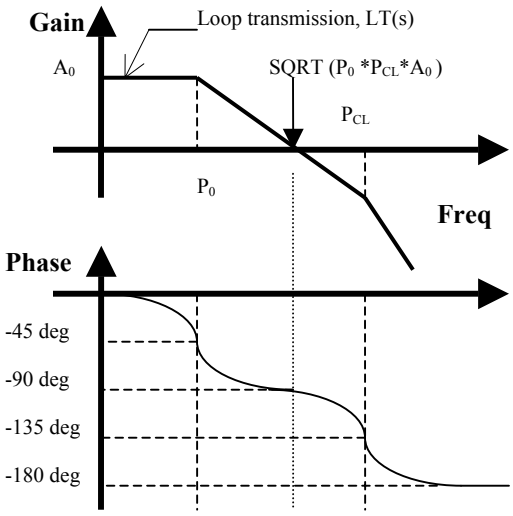

Figure 9 Operational amplifier loop transmission gain and phase for $p_0 < \omega_{LTu} < p_{CL}$

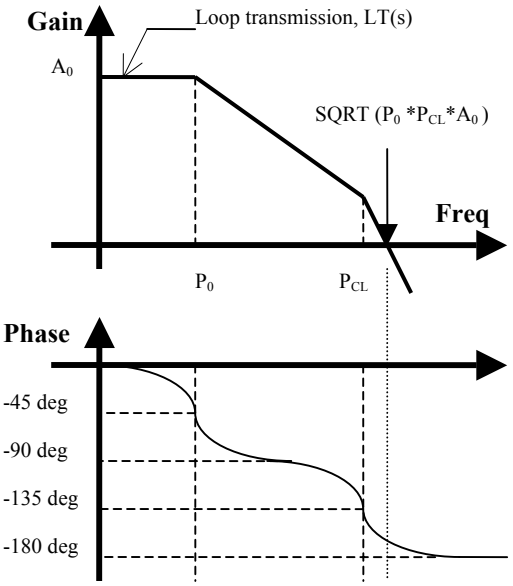

Figure 10 Operational amplifier loop transmission gain and phase for $p_0 << p_{CL} < \omega_{LTu}$

If the loop transmission unity gain frequency is greater than both poles, $p_0 << p_{CL} < \omega_{LTu}$, it means that: $p_0 A_0 > p_{CL}$. Again, this can be determined from equation (40). In this case the square root term in parenthesis, in equation (44), is positive and less than one. Therefore the phase can be in the range of $\varphi \in (-135\deg \div -180\deg)$. That is bad, it means that the operational amplifier could oscillate. In Figure 10 there is a graphical representation of the pole locations and phase with respect to loop transmission unity gain frequency.

The solution to driving large capacitive loads

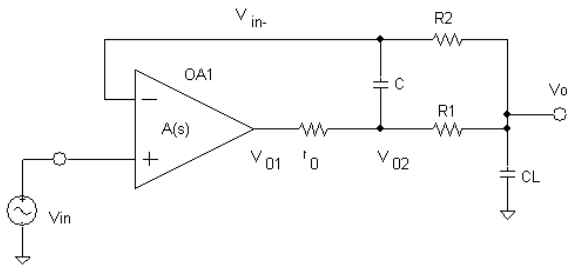

Figure 11 Capacitive load driver

The circuit in Figure 11 shows a clever topology that can extend the capability of a regular operational amplifier to drive larger capacitive loads. Although the circuit adds two resistors and one capacitor, the mathematical analysis is not trivial. Consequently, many designers prefer to copy an existing design that has being proved to be stable for a specific configuration.

A simple analysis of the circuit shows that the addition of capacitor C from the output to the inverting input counteracts the phase shift due to capacitive load CL.

In other words, the pole due to capacitor CL is annihilated by the zero introduced by the capacitor C.

In order to determine the transfer function of this circuit we can write the following equations:

$$V_{01} = (V_{in} - V_{in-}) * A(s) \quad (45)$$

$$\frac{V_{01} - V_{02}}{r_0} = \frac{V_{02} - V_0}{R_1} + (V_{02} - V_{in-}) * sC \quad (46)$$

$$(V_{02} - V_{in-}) * sC = \frac{V_{in-} - V_0}{R_2} \quad (47)$$

$$V_0 * sC_L = \frac{V_{02} - V_0}{R_1} + \frac{V_{in-} - V_0}{R_2} \quad (48)$$

The set of above four equations, (45) through (48) can be solved to extract the ratio V_0 / V_{in}, which represents the transfer function. The transfer function is shown in the following equation:

$$\frac{V_0}{V_{in}}(s) = \frac{A(s) * \frac{1 + sC*(R_1 + R_2)}{(1 + sC_L r_0) * [1 + sC*(R_1 + R_2)] + sC_L R_1 * (1 + sCR_2)}}{1 + \left[1 + \frac{s^2 CC_L R_1 R_2}{1 + sC*(R_1 + R_2)}\right] * A(s) * \frac{1 + sC*(R_1 + R_2)}{(1 + sC_L r_0) * [1 + sC*(R_1 + R_2)] + sC_L R_1 * (1 + sCR_2)}} \quad (49)$$

Although equation (49) is complex one interesting feature can be extracted that might help understand how this circuit works. If the capacitive load is very small, for instance CL = 0, the entire equation becomes equal to equation (32), which is the basic transfer function of a non-inverting unity gain buffer. In this case, capacitor C and the additional resistors R1 and R2 are totally transparent. This means that the contribution of C, R1 and R2 is only activated by the presence of the load capacitor CL.

Comparing equation (32) and (49) we can extract a few components:

The feedback factor β:

$$\left[1 + \frac{s^2 CC_L R_1 R_2}{1 + sC*(R_1 + R_2)}\right] \quad (50)$$

Open loop gain:

$$A(s) * \frac{1 + sC*(R_1 + R_2)}{(1 + sC_L r_0) * [1 + sC*(R_1 + R_2)] + sC_L R_1 * (1 + sCR_2)} \quad (51)$$

The loop transmission equation is computed by multiplying equations (50) and (51). Rearranging terms we have the following equation:

$$LT(s) = A(s) * \frac{1 + sC*(R_1 + R_2) + s^2 CC_L R_1 R_2}{1 + sC*(R_1 + R_2) * \left(1 + \frac{C_L}{C} * \frac{r_0 + R_1}{R_1 + R_2}\right) + s^2 CC_L R_1 R_2 * \left(1 + r_0 * \frac{R_1 + R_2}{R_1 R_2}\right)} \quad (52)$$

If we ignore for the moment the output resistance of the operational amplifier, $r_0 = 0$, the loop transmission becomes:

$$LT(s) = A(s) * \frac{1 + sC*(R_1 + R_2) + s^2 CC_L R_1 R_2}{1 + sC*(R_1 + R_2)*\left(1 + \frac{C_L}{C} * \frac{R_1}{R_1 + R_2}\right) + s^2 CC_L R_1 R_2} \quad (53)$$

The second term in equation (53) is the transfer function of a parametric equalizer that always introduces a notch. Equation (53) can be written again as follows:

$$LT\ (s) = A\,(s) * \frac{\omega_1^{\ 2} + s * \frac{\omega_1}{Q} + s^2}{\omega_1^{\ 2} + s * \frac{\omega_1}{Q} * k + s^2} \quad (54)$$

where

$$\omega_1 = \frac{1}{\sqrt{CC_L R_1 R_2}} \quad (55)$$

$$Q = \sqrt{\frac{C_L}{C}} * \frac{\sqrt{R_1 R_2}}{R_1 + R_2} \quad (56)$$

$$k = 1 + \frac{C_L}{C} * \frac{R_1}{R_1 + R_2} \quad (57)$$

In order to keep the loop transmission as smooth as possible, the k factor needs to be as close as possible to one. This means that:

$$C*(R_1 + R_2) >> C_L * R_1 \quad (58)$$

The notch in the loop transmission affects the phase also by pushing the closer to –180 deg. It is good practice to increase the notch frequency above the unity gain of function A(s), which is (p_0 * A_0). A rule of thumb is to design the notch frequency at least 20% higher.

If the output resistance of the operational amplifier is taken into consideration, then the frequency response of the parametric equalizer is not that clean, since the low pass, denominator in (53) is shifted down in frequency with respect to the high pass, nominator in equation (53). In this case the loop transmission has a ripple in the frequency response rather than a notch. The resonant frequency of the low pass is:

$$\omega_2 = \frac{1}{\sqrt{CC_L R_1 R_2 * \left(1 + r_0 * \frac{R_1 + R_2}{R_1 R_2}\right)}} \quad (59)$$

Again, to keep all these disturbances above the unity gain frequency of the loop transmission, we to set the following conditions:

$$p_0 A_0 << \omega_2 \quad (60)$$

which means:

$$p_0 A_0 * \sqrt{CC_L R_1 R_2 * \left(1 + r_0 * \frac{R_1 + R_2}{R_1 R_2}\right)} << 1 \quad (61)$$

Another design formula but not as critical is to keep factor k as close as possible to one. This means:

$$C*(R_1 + R_2) >> C_L * (r_0 + R_1) \quad (62)$$

If the output resistance r_0 is not known we can assume an average value of 75 Ω.

Formulae (61) and (62) are design guides for the capacitive load driver shown in Figure 11. The designer can set either one resistor and determine the other components or set the capacitor and determine resistor values.

4. CONCLUSION

The paper presented several analog circuits commonly used in the professional audio applications. A group of three line receivers were analyzed from the functional point of view with mathematical demonstrations. Real life applications were considered to reveal the capability of each circuit to maintain its performance. It was shown that only the high common mode input impedance line receiver could hold the common mode rejection specification under ideal and non-ideal

conditions. The formulae presented in this section provide the designer good guidelines for topology and component value selection. The last section presented a ubiquitous ADC driver that is difficult to analyze. Although it has only four or five components, the mathematical description of the circuit functionality is complex. Formulae were derived to assist the designer with proper component type and value selection.

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