# What's a PTAT Temp. Coefficient, & Where Does It Come From?

## Introduction

THAT Corporation's VCAs and RMS detectors exhibit temperature coefficients that are proportional to absolute temperature (PTAT). This fact is occasionally disconcerting to some users, but is rarely an issue in audio applications. When it is an issue, it is relatively easy to compensate and, in some cases, the coefficients of the RMS detector and VCA cancel each other.

This temperature coefficient is due to fact that, in both the RMS and VCA topologies, the outputs rely on transistors that may be operating at different currents. The collector current of a transistor can be expressed as

$$i_C = I_S\, e^{(\frac{v_{BE}}{V_T})}$$

(One might want to review Microelectronic Circuits, by Sedra and Smith, or any other suitable textbook with a college level introduction to electronics)

Taking the log of both sides,

$$\ln i_C = \ln I_S + \frac{v_{BE}}{V_T}$$

which can be rearranged to yield

$$\frac{v_{BE}}{V_T} = \ln(\frac{i_C}{I_S})$$

If we wish to find the delta $V_{BE}$ of two transistors running at different currents,

$$\frac{\Delta v_{BE}}{V_T} = \ln(\frac{i_{C1}}{I_S}) - \ln(\frac{i_{C2}}{I_S}) = \ln\left(\frac{\frac{i_{C1}}{I_S}}{\frac{i_{C2}}{I_S}}\right) = \ln\left(\frac{i_{C1}}{i_{C2}}\right)$$

which yields

$$\Delta_{v_{BE}} = V_T \ln(\frac{i_{C1}}{i_{C2}}) = \frac{kT}{q} \ln(\frac{i_{C1}}{i_{C2}})$$

Since k and q are both constants, we can see that for a given pair of currents, the magnitude of $\Delta V_{BE}$ is directly proportional to T. At this point, it's worth noting that since the highly temperature dependent term $I_S$ has been canceled, all of the $\Delta V_{BE}$'s remaining temperature dependence is in the $V_T$ term.

## So what does this all mean?

Let's first look at the RMS detector. Figure 1, which is also Figure 3 in the THAT 2252 Datasheet, shows a macro-model of the THAT 2252, a true-rms detector. The input is a

 

virtual ground, and the input resistor acts to convert the input voltage to a current. The first stage is a current mode, full wave rectifier (an absolute value circuit). The second stage uses the base-emitter junctions of two transistors to log and double the input current. Doubling the signal while logged is equivalent to squaring it. This stage is followed by a log filter that averages the signal, thus performing the mean calculation of the rms function. A subsequent stage provides buffering and offset cancellation. The square root is calculated implicitly at the VCA's exponential control port.

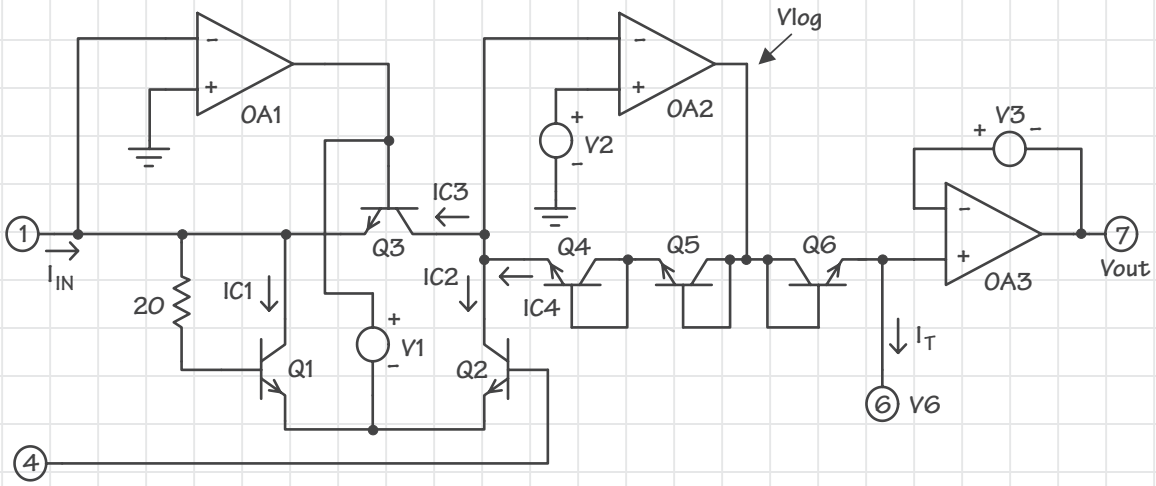


Figure 1. Simplified Internal Diagram

In this model, transistors Q1, Q2, and Q3, V1, and OA1 form the current mode rectifier. During the positive half cycle, the output of OA1 (through V1) turns Q1 "on", and the current through this transistor servo's the inverting input of OA1 to ground. This feedback current is mirrored by Q2, and drawn from the log amp. During the negative half cycle , feedback current is supplied directly to the input from the log amp by Q3, while V1 turns Q1 and Q2 off. Being inside the feedback loop of OA1, the temperature coefficients of Q1, Q2, and Q3, and V1 are nullified.

Q4 and Q5, V2, and OA2 comprise the next stage, which is a log amplifier. V2 is a diode-connected transistor driven with a fixed current ($I_{Bias1}$) that biases OA2 a diode drop above ground for the purpose of keeping Q3 out of saturation. Q4 and Q5 both run at a signal dependent current.

At the point labeled Vlog, the signal is nominally 3 $V_{BE}$ drops above ground. One of these drops is canceled by Q6, which is the log filter diode. This diode runs at a fixed DC current which is set by the current programmed for $I_T$. V3 is effectively a pair of current-source-biased (at $I_{Bias2}$), diode-connected transistors that provided the final two $V_{BE}$ drops worth of offset cancellation.

Q4, Q5, and Q6, as well as the diode-connected transistors in V2 and V3 have different areas (and thus different scale currents [$I_S$]) and are running at different currents, and it may not be intuitively clear why, when the detector is at its zero dB reference level, the PTAT coefficient is nullified. We define the zero dB reference level as being the input signal level that results in zero


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volts out of the detector, which implies that the magnitude of the forward diode drops going up must equal that of the diode drops used as cancellation. Let's define these as

$$V_{Up} = V_T \ln\left(\frac{I_{Bias1}}{I_S A_1}\right) + 2V_T \ln\left(\frac{I_{Signal}}{I_S A_2}\right) \text{ and}$$

$$V_{Down} = V_T \ln\left(\frac{I_T}{I_S A_3}\right) + 2V_T \ln\left(\frac{I_{Bias2}}{I_S A_4}\right)$$

Since we know the two voltages must be equal at the zero dB reference level,

$$V_T \ln\left(\frac{I_{Bias1}}{I_S A_1}\right) + 2V_T \ln\left(\frac{I_{Signal\,0}}{I_S A_2}\right) = V_T \ln\left(\frac{I_T}{I_S A_3}\right) + 2V_T \ln\left(\frac{I_{Bias2}}{I_S A_4}\right)$$

$$V_T \ln\left[\frac{I_{Bias1}(I_{Signal\,0})^2}{(I_S)^2 A_1 \times A_2}\right] = V_T \ln\left[\frac{I_T (I_{Bias2})^2}{(I_S)^2 A_3 \times A_4}\right]$$

Canceling the terms common to both sides leaves

$$\left[\frac{I_{Bias1}(I_{Signal\,0})^2}{A_1 \times A_2}\right] = \left[\frac{I_T (I_{Bias2})^2}{A_3 \times A_4}\right]$$

We can then say

$$I_{Signal\,0} = \sqrt{\frac{I_{Bias1} \times I_T (I_{Bias2})^2}{A_1 \times A_2 \times A_3 \times A_4}}$$

Note that there are no temperature dependent terms in the equation. As previously mentioned, the PTAT coefficient is entirely a function of $V_T$, and cancellation of this term is indicative of the zero temperature coefficient that results at the zero dB reference level. This holds true as long as all of the devices are at equal temperature, and the currents are low enough that parasitic impedances don't cause significant errors in the forward drop.

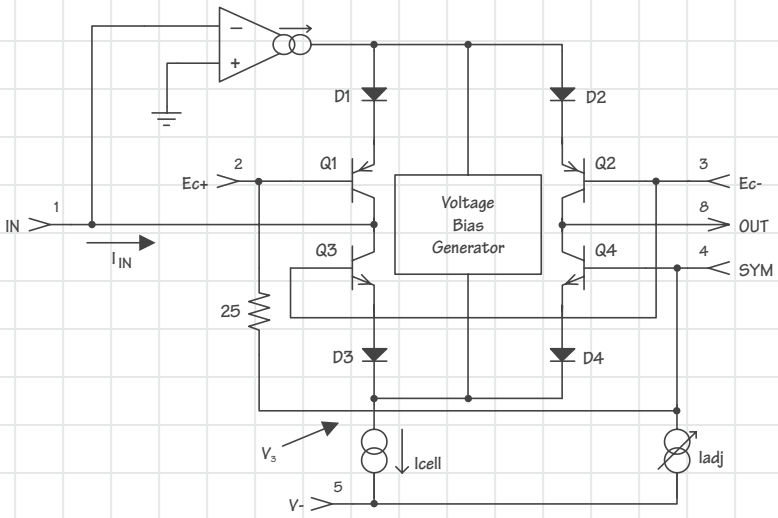


Figure 2. THAT 2181 VCA

Figure 2 is actually Figure 5 from the THAT 2181 datasheet, and shows a macro-model of a typical log/anti-log VCA. In this case, we'll avoid the excruciating detail, and give the reader a simple, intuitive explanation. Interested readers may want to peruse Gary Hebert's paper, An Improved, Monolithic Voltage-Controlled Amplifier, presented at the 99th AES Convention in New York, for a more detailed explanation of VCAs.

 

*Consider only large, negative going input signals. One can see that Q1 (along with the diode connected transistor in series with it) and the input amplifier act as a log amplifier, logging the input current. Q2 (and its associated series diode connected transistor), in conjunction with the external output amplifier, acts as an anti-log amplifier, returning the signal to the linear domain. Q3 and Q4 (and their associated series diode connected transistors) handle positive going signals in a similar manner. The voltage bias generator biases the gain cell Class AB, keeping crossover distortion to a minimum. Gain is changed by adding a DC gain control signal to the logged input signal.*

*Given the case where the input current equals the output current (zero dB gain), it should be apparent that the $V_T$ terms for the input side of the gain cell will be canceled by those on the output side of the gain cell. The resulting equation is nearly identical to that derived for a pair of diodes in the introduction,*

$$\Delta_{V_{BE}} = V_T \ln\left(\frac{i_{C_{In}}{}^2}{i_{C_{Out}}{}^2}\right)$$

*but with the current ratio squared. This results from the fact that the series diode connected transistors add with Q1 - Q4, and adding in the log domain is, of course, multiplication, and since the currents are equal, these currents are squared. We can see by inspection that when the currents are equal, $V_T$ is multiplied by the natural log of one, which is zero, so there is no effect due to $V_T$. As the ratio varies away from one, the effect of the PTAT term in $V_T$ becomes more pronounced.*

*For curiosity's sake, one could rearrange this equation to find the voltage gain*

$$A_V = \frac{I_{Out}}{I_{In}} = \sqrt{e^{\frac{-\Delta V_{BE}}{V_T}}} = e^{\frac{-\Delta V_{BE}}{2 \times V_T}}$$

*or the gain in dB*

$$G_{dB} = 20 \log\left(e^{\frac{-\Delta V_{BE}}{2 \times V_T}}\right) = 10 \log e^{\frac{\Delta V_{BE}}{V_T}} = \frac{20 \times \Delta V_{BE}}{2 \times V_T} \log(e) = \frac{0.4343 \times 20 \times \Delta V_{BE}}{2 \times V_T}$$

*(Note that $\Delta V_{BE}$ equals $E_{C+}$ -($E_{C-}$))*

$$G_{dB} = 4.343 \times \frac{\Delta V_{BE}}{V_T} \quad Or \quad 167.04 \times \Delta V_{BE} \; @ \; T=300^\circ K$$

*By observation we can see that gain control is linear in dB and inversely proportional to T in degrees Kelvin. We can calculate the required gain control voltage to be*

$$V_{ControlVoltage} = \Delta V_{BE} = \frac{V_T \times G_{dB}}{4.343} = 0.0061 \times G_{dB} \quad At\ T = 300^\circ K$$


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