

VCA's in a pan potentiometer application

The pan potentiometer (pan pot) allows users to steer an audio signal between two channels and, unlike standard potentiometers which have a linear taper, or audio potentiometers which have something like a log taper, the elements in a pan pot will have something approximating a sin vs. cos taper. The intent is to yield a constant power sum of the two output channels as the pan control is swept.

The common method of implementing a pan pot, using a single linear potentiometer with the wiper grounded, and resistors of approximately equal value to the pan pot connected appropriately, approximates the sin vs. cos taper described earlier. While this is certainly an elegant solution, there is no easy way to automate this arrangement, short of a motorized potentiometer, for pro-audio applications. "Digi-pots" would introduce significant amounts of zipper noise, and have limited adjustability as well.

The following schematic shows how an "electronic pan pot" can be implemented. The cosine law of the pan pot is implemented by a nonlinear circuit with two break points. U4A&B are the control voltage buffers for the VCAs, U1 and U2 respectively. One VCA is driven via its E_c - control port while the other is driven via its E_c+ port. This allows a single polarity of control signal to increase the gain of one VCA while decreasing the gain of the other. U3A&B are the respective output amplifiers for U1 and U2. U5A&B are used for breakpoint generation.

The VCA and control voltage buffer portions of this schematic are similar to other application circuits, and the usual precautions apply; use a low noise, wideband amplifier for the control voltage buffer to minimize noise modulation and the potential for instability, etc. U4A scales the 0-5 V control signal so that at zero volts, U1's gain is zero dB, and as the control voltage increases, the gain goes down. U4B performs similar a similar scaling, but R1B offset the control signal so that U2 is essentially off at a control voltage of zero, but increases to a gain of zero dB when the control voltage is 5 V.

U5 is the breakpoint generator. U5B scales and offsets the 0-5 V control to approximately ± 0.6 V, as well as inverting the polarity. It is easiest to understand the breakpoint circuitry by looking at one half of the circuit at a time. While the 0-5V control signal is below 2.5 V, the output of U5A is negative, and D4 is off. Since pin 2 of U5A and pin 2 of U4A are both at zero volts, there is no current through R6 and R8, and the output of U4A is purely a function of the 0-5 V control signal via R9 and R13. As this signal goes above 2.5 V, the output of U5A goes positive, D4 conducts, and the breakpoint generator begins to affect the output of U4A. While the output of U5B is significantly more positive than -0.5 V, the gain of U5A is two, and its affect on the $ec-$ of the VCA is to approximately double the slope of the control signal. As the output of U4B continues to approach -0.6 V, D1 begins to turn on, and the gain of U5A begins to increase rapidly. This results in the second breakpoint.

The operation of the other half of the circuit is basically the same, but all of the breakpoints occur below the 2.5 V at the input. The results, given in figure 2, show the gain of right and left channels, which correspond to U1 and U2 as a function of control signal and temperature. As the second breakpoint kicks in, there is a distinct gain error as a function of temperature. This turns out to be relatively insignificant.

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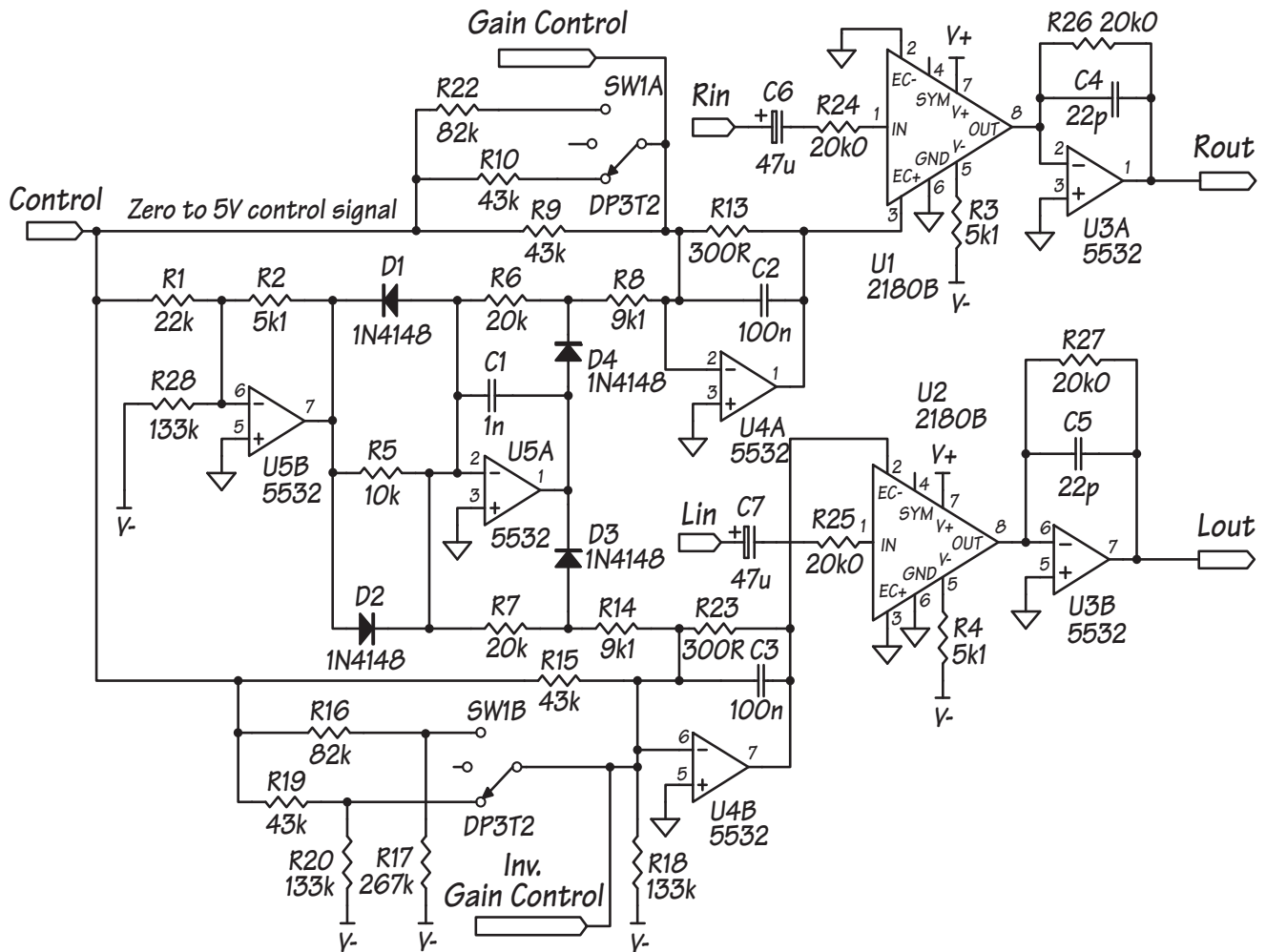


Figure 1: Pan pot circuit

Figure 3 shows the deviation from ideal constant power summing. Note that the vertical axis is in dB. This result is calculated with the equation:

$$\text{error} = 20 \times \log \left(e^{\frac{E_c - \text{gain}}{V_T}} + e^{\frac{E_c + \text{gain}}{V_T}} \right), \text{ since the gain for either channel is } e^{\frac{E_c}{V_T}}$$

As the graph shows there is less than 1 dB deviation from ideal, and the temperature errors so prominent in Figure 2, have minimal impact on the gain error, because they occur when the gain of a particular channel is significantly below that of the more prominent channel. SW1 provides a means for shaping the gain at the midpoint. Putting equal value resistors in parallel with R9, R15, and R19 will lower the gains at the midpoint to -6 dB, while putting double their value in parallel will lower the gain at the midpoint to -4.5 dB.

All of the results shown are based on ideal values of components and exact values of the supplies and reference. For a given "real world" application, the designer may need tighter tolerances on components, and to generate an accurate, stable negative reference for generating offsets.

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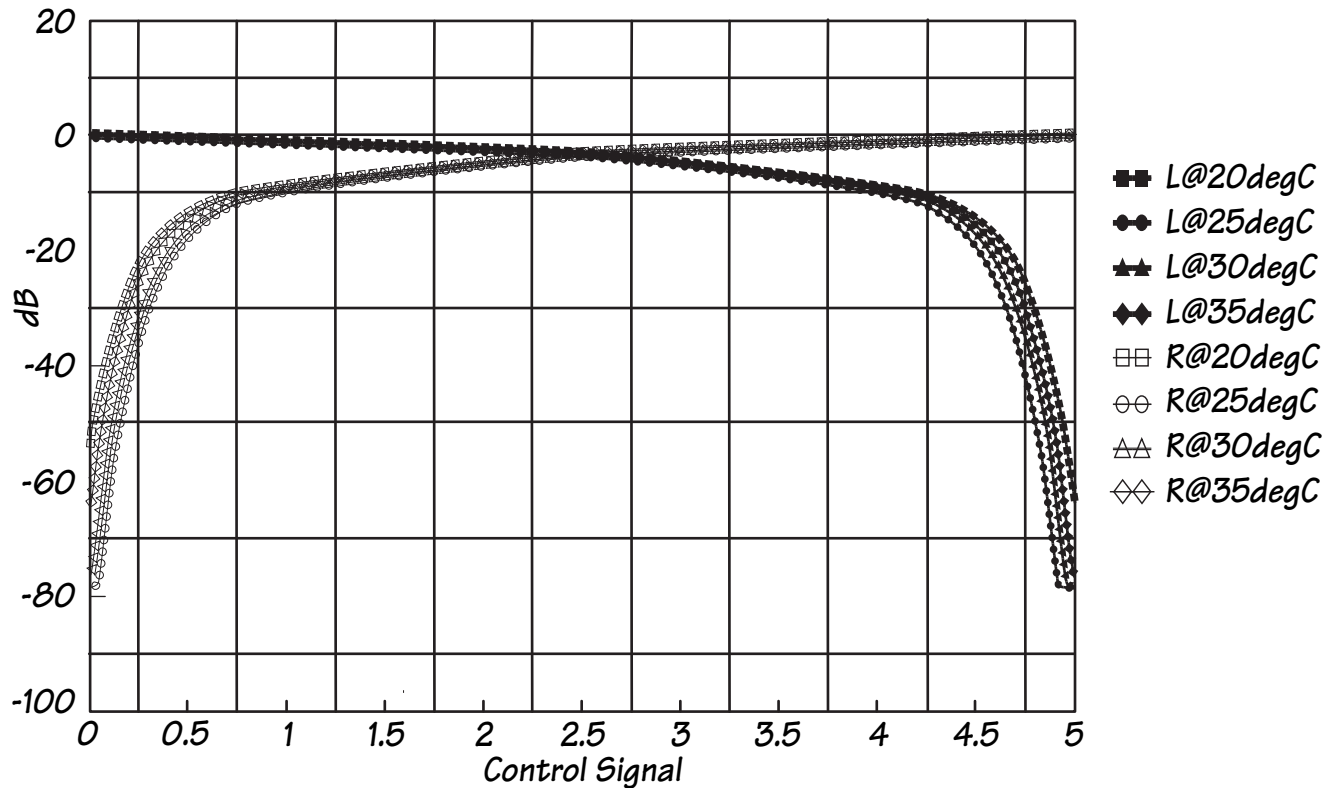


Figure 2: VCA gain as a function of control signal

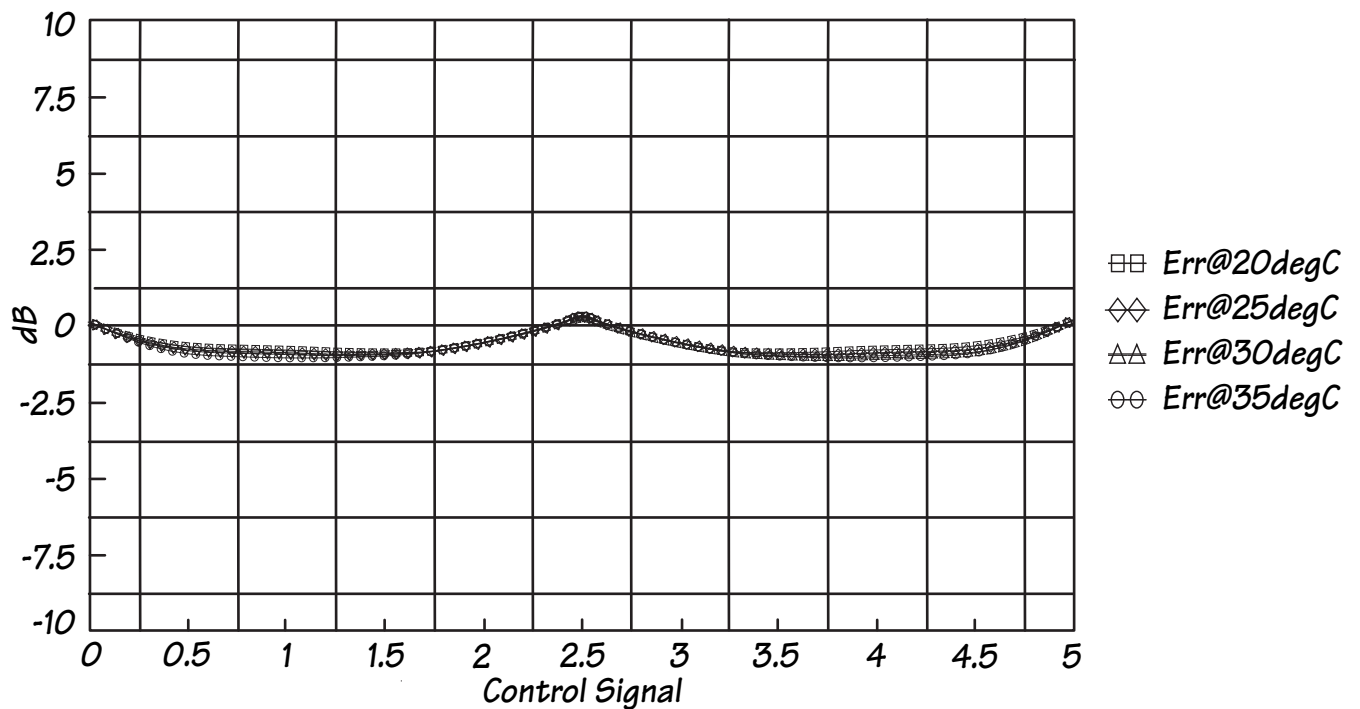


Figure 3: Gain error with respect to constant power summing