

A Fully Adjustable Noise Gate

The circuits within this application note feature THAT4301 Analog Engine® to provide the essential elements of voltage-controlled amplifier (VCA) and rms-level detector (RMS). Since writing this note, THAT has introduced several new models of Analog Engines, as well as new VCAs. With minor modifications, these newer ICs are generally applicable to the designs shown herein, and may offer advantages in performance, cost, power consumption, etc., depending on the design requirements. As well, a standalone RMS is available to complement our standalone VCAs. We encourage readers to consider the following alternatives in addition to the 4301:

- Low supply voltage and power consumption: 4320
- Low cost, supply voltage, and power consumption: 4315
- Low cost and power consumption: 4305
- High-performance (VCA only): 2180-series, 2181-series
- Dual (VCA only): 2162
- RMS (standalone): 2252

For more information about making these substitutions, please contact THAT Corporation's technical support group at apps_support@thatcorp.com.

THAT Corporation

45 Sumner St, Milford, MA 01757-1656 USA; www.thatcorp.com; info@thatcorp.com

Gates are useful for suppressing background noise in the absence of masking source material, but for a gate to sound "natural", it can be desirable to control one or more of the following parameters:

- the threshold below which the gate acts;
- the hold time which prevents gating action during brief pauses in the source material;
- the release rate during which the gain is smoothly "faded" down.

The circuit shown in Figure 1 is a feedforward design with independent, variable control of each gating parameter. Gates need to react quickly to be effective, so the level detector timing must be very fast. A fast detector, however, results in ripple on its output waveform. Ripple, in turn, can cause "false" triggering of the gate when the detector output is very near the trip point of the threshold comparator.

A solution is to use a timing circuit we refer to as the "non-linear capacitor" or "NLC", shown in Figure 1 around OA2. This circuit utilizes the Miller Effect to amplify the effect of C6 while the change in the voltage at pin 5 is small enough to avoid turning on D1 or D2. When these devices do turn on, the gain of OA2 is reduced and the contribution of C6 is only 100nF. The exact tuning of the NLC is best done by ear, but there is an in-depth explanation of this circuit, which includes some rough guidelines for tuning, at the end of THAT Corporation's Design Note 03 (formerly Application Note 103). We suggest reviewing that document before beginning to tweak the circuit's performance.

Q1 and Q2 form logarithmically adjustable current sources, and Q3 sets their full-scale currents. The rest of the design is relatively straightforward. The current through Q3 is the program current, and it sets up a voltage across Q3's base-emitter junction. When VR4 and VR5 are adjusted to put this same voltage on their VBE's, they will have the same program current running through them. The potentiometers allow the individual transistors currents to be adjusted, and as a result of the logarithmic nature of transistors, the current will vary by a factor of 10 for each 60mV change in VBE. The divider networks on each adjustment limit the dynamic range of the controls, since a $VBE = 0.6V$ divided by 60mV/decade yields a range of 10 decades, much too large in practical terms.

U2A and U2B are connected as comparators, with VR3 providing a means for adjusting the threshold. While the signal is above threshold, the LM393 steals all the current from Q1, and the output of U2B is forced low. In the steady state condition, the output of U3A (we used a FET input op-amp) will be high. VR1 is used to trim the output of U1D to yield a VCA gain of one.

When the signal level drops below threshold, the output of U2A become a high impedance, and the current in Q1 causes the voltage on C4 to ramp upwards. After a time, which is directly proportional to the current in Q1, the comparator, U2B, trips and its output becomes a high impedance, allowing the integrator, U3A, to ramp down at a rate that is directly proportional to the current in Q2. This is how the release rate is set.

