

Verilog® Encoder Code for Broadcast Applications

FEATURES

- Verilog-based BTSC encoder solution
 - Broadcast quality
 - Realizable in small footprint
 - All digital
- Complete BTSC baseband generator
 - Stereo
 - SAP
 - 4.5 MHz aural or baseband output
- Well-documented Verilog HDL
- Evaluation board and reference design based on Xilinx gate array technology

APPLICATIONS

- Professional TV broadcast equipment
 - Modulators
 - BTSC encoders
 - Digital to analog TV conversion equipment

Description

CATV/broadcast equipment makers are facing new challenges and seeing new opportunities for smaller BTSC encoding solutions as cable operators both expand their VOD deployments and continue their migration to digital.

THAT Corporation's Verilog-based pro encoder solution is ideally suited to address these market conditions. It provides the complete suite of BTSC encoding functions, meets the performance demands of high-end broadcast applications, and can be realized in a small footprint.

The solution can be configured to generate a 4.5MHz aural carrier and/or baseband BTSC signal from L/R and SAP inputs. The extensive set of BTSC Encoder functions performed, include:

- L+R and L-R matrix 75 μ sec pre-emphasis

- BTSC compression
- Pilot generation
- 4.5 MHz aural carrier modulation
- L-R 2fH amplitude modulation and SAP 5fH frequency modulation

The encoder comes with an extensive set of deliverables including well commented source code, an FPGA-based evaluation board, and complete engineering support including customization and evaluation services.

The system is offered for a license issue fee plus per-instance royalties. Code meeting the specifications shown in this data sheet is available immediately. Our engineers are implementing additional features and performance improvements, so please check our web site for the latest updates.

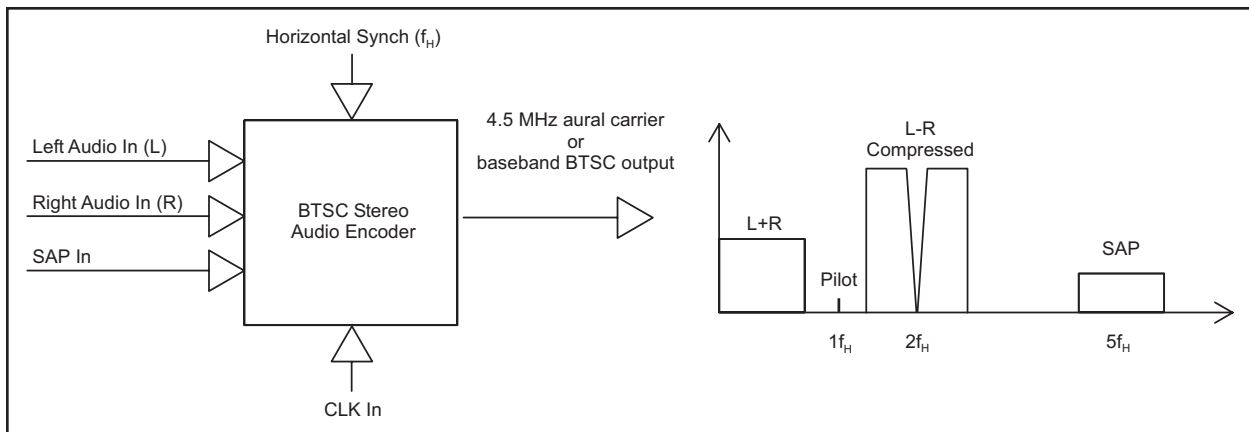


Figure 1. BTSC Stereo encoder block diagram

SPECIFICATIONS

<u>I/O</u>	
<p style="text-align: center;"><u>Inputs</u></p> <ul style="list-style-type: none"> • Four signal serial interface to Stereo A/D (similar to I²S interface) • SAP A/D Interface • Horizontal synch input • System clock input • Mode configuration <ul style="list-style-type: none"> – Stereo / mono – SAP off / on – Test modes • Reset input 	<p style="text-align: center;"><u>Outputs</u></p> <ul style="list-style-type: none"> • D/A interface to support clock and data output for 4.5 MHz carrier • D/A interface to support clock and data output for baseband

Performance Specifications³

Parameter	Conditions	Typical
Stereo Separation	50Hz - 500Hz @ 10% EIM ²	49 dB
	500Hz - 5kHz @ 10% EIM ²	44 dB
	5kHz - 14kHz @ 10% EIM ²	32 dB
Stereo THD+N	1 kHz, 100%, NR on, 8 kHz BW	0.2 %
Stereo S/N	No tone, NR on, 15 kHz BW	80 dB
Stereo Frequency Response	50 - 14 kHz	± 0.1 dB
SAP THD+N	1 kHz, 100%, NR on, 10 kHz BW	0.6 %
SAP S/N	No tone, NR on, 10 kHz BW	90 dB
SAP Frequency Response	50 - 10 kHz	± 0.4 dB

System Component Requirements

Component	Description
Xilinx Spartan3 FPGA	XC3S400-4FG456C (or similar package) for applications requiring baseband output only. XC3S1000-4FG456C (or similar package) for aural or simultaneous aural/baseband outputs.
Oscillator	24.576 MHz
A/D for Stereo	16 bits, 48 kHz sample rate

¹ This product is covered by one or more of the following U.S. patents and corresponding filings worldwide: 5,796,842 6,037,993 6,118,879 6,192,086 6,259,482 6,588,867. Other patents pending.

² 75 μ s equivalent input modulation (EIM): The audio signal level prior to encoding that results in a stated percentage modulation when the encoding process is replaced by 75 μ s pre-emphasis.

³ Based on 4.5 MHz aural carrier output

System Component Requirements (continued)	
Component	Description
A/D for SAP	Same as above.
D/A for aural or baseband output	TI DAC904E (or similar that supports 14 bits, 24.576 MHz sample rate). Providing simultaneous aural and baseband outputs would require another identical D/A.
Horizontal sync stripper	Circuitry shown in reference design.
Minor discrete components	Shown in reference design.
Flash memory (optional)	XCF08PVO48C. Other FPGA configuration schemes are possible.

Applications Assistance

The BTSC encoder solution comes with the following comprehensive set of deliverables:

- An evaluation board, based on Xilinx gate-array technologies, for performing an engineering assessment of THAT's BTSC encoder functional block.
- Well documented/commented Verilog source code.
- All files associated with simulation, synthesis, placement, and routing.
- Functional test wrapper.

THAT provides a range of system integration support for customers. The standard support package includes the following:

- General applications assistance
- A/D & D/A converter selection assistance
- Encoder interface customization
- Final design evaluation

NOTES: