

Verilog® Decoder Code for Integrated Circuits

FEATURES

- Complete BTSC decoder
 - Stereo
 - SAP
 - Optional 4.5 MHz aural carrier FM demodulator
 - All digital
 - Synthesizes into FPGA or ASIC
- Well-documented Verilog HDL
 - Efficient design
 - Optimized for consumer applications
- Selectable sample rates
 - 32, 44.1, & 48 kHz outputs
- Evaluation board based on Xilinx gate-array technology

APPLICATIONS

- Consumer multimedia products
 - LCD TVs
 - Cable/satellite set tops
 - DVD recorders
 - Digital TVs
 - PVRs/DVRs
 - PC TV tuner cards

Description

THAT Corporation's Verilog-based decoder FM demodulates a 4.5 MHz aural signal and expands the resultant BTSC signal into L/R and SAP outputs. This low-cost, gate-efficient BTSC decoder is ideally suited to enable BTSC decoding from within TVs, set-tops, DVD recorders, PVRs/DVRs, and other TV-centric, consumer products.

THAT's BTSC Decoder performs the full suite of BTSC Decoder functions, including:

- Pilot recognition
- L-R $2f_H$ amplitude demodulation and SAP $5f_H$ frequency demodulation
- 75 μ sec de-emphasis
- BTSC expansion

- L+R and L-R matrix

THAT offers a range of solutions at various levels of complexity, in order to allow users to trade off complexity against performance, from consumer to broadcast grade.

The decoder comes with an extensive set of deliverables including well commented source code, an FPGA-based evaluation board, and complete engineering support including customization and evaluation services.

The system is offered for a license issue fee plus per-instance royalties. Code meeting the specifications shown in this data sheet is available immediately. Our engineers are implementing additional features and performance improvements, so please check our web site for the latest updates.

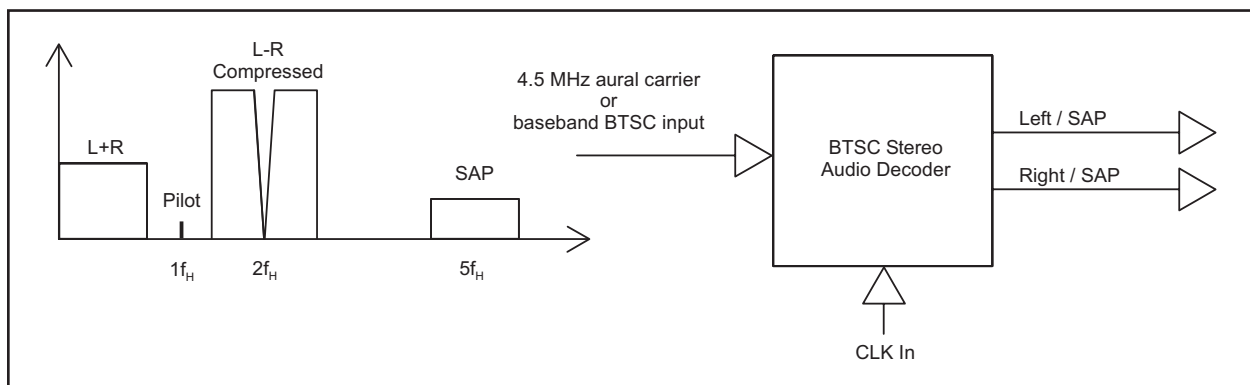


Figure 1. BTSC Stereo decoder block diagram

SPECIFICATIONS

<u>Inputs</u>	<u>I/O</u>	<u>Outputs</u>
<ul style="list-style-type: none"> • 4.5 MHz aural carrier or baseband BTSC input • System clock input • Mode configuration <ul style="list-style-type: none"> – Stereo / mono – SAP off / on – Test modes • Reset input 		<ul style="list-style-type: none"> • D/A interface to support clock and data • L / SAP • R / SAP • Stereo/SAP signal indicators

<u>Electrical Specifications</u>		
Parameter	Conditions	Typical
D/A	32/44.1/48 kHz sample rate	16 bits
A/D (Baseband)	264.6/288 kHz sample rate	16 bits
A/D (4.5Mhz aural)	16.9344/18.432 MHz sample rate	10 bits
Horizontal Synch Rate		15.734 kHz
System Clock Rate		97 x A/D ² Hz
Estimated ASIC Gate Count	Stereo + SAP	58 k Gates
	Stereo + SAP + 4.5MHz Demod.	71 k Gates
PLL Lock Time	Pilot moved by 10Hz	120 ms
Pilot Frequency range		15.664 - 15.803 kHz
Pilot Deviation Threshold		User Defined
Stereo Separation	50 - 12 kHz, NR on	
	1% EIM ³	21 dB
	10% EIM ³	24 dB
	66% EIM ³	25 dB
Stereo THD+N	1 kHz, 100%, NR on, 12 kHz BW	0.2 %
Stereo S/N	No tone, NR on, 15 kHz BW	84 dB
Stereo Frequency Response	50 - 12 kHz	± 0.3 dB
Mono THD+N	1 kHz, 100%, emphasis on, 12 kHz BW	0.04 %
Mono S/N	No tone, emphasis on, 15kHz BW	80 dB
Mono Frequency Response	50 - 12 kHz	± 0.14 dB

1 This product is covered by one or more of the following U.S. Patents, Applications and corresponding filings worldwide: 6,037,993 6,192,086 6,259,482, 60/370,064, 60/555,853, 60/602,169. Other patents pending.

2 Base-band A/D

3 75 μ s equivalent input modulation (EIM): The audio signal level prior to encoding that results in a stated percentage modulation when the encoding process is replaced by 75 μ s pre-emphasis.

Electrical Specifications (continued)		
Parameter	Conditions	Typical
SAP THD+N	1 kHz, 100%, NR on, 9 kHz BW	0.5 %
SAP S/N	No tone, NR on, 10 kHz BW	84 dB
SAP Frequency Response	50 - 9 kHz	± 0.4 dB
SAP Deviation Threshold		User Defined

Applications Assistance

The BTSC decoder solution comes with the following comprehensive set of deliverables:

- An evaluation board, based on Xilinx gate-array technologies, for performing an engineering assessment of THAT's BTSC decoder functional block
- Well documented/commented Verilog source code
- All files associated with simulation, synthesis, placement, and routing
- Functional test wrapper

THAT provides a range of system integration support for customers. The standard support package includes the following:

- General applications assistance
- A/D & D/A converter selection assistance
- Decoder interface and performance customization
- Final design evaluation

NOTES: